Performance Analysis of Single-Multiplier Digital Sine-Cosine Generators

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Abstract

In this paper, second order structures satisfying single-multiplier digital sine-cosine generators are derived analytically, resulting in four different realizations. Some important characteristics of these generator structures, like total harmonic distortion percentage (*THD*%), frequency error (f_1error) and frequency resolution (Δf) are defined and examined as performance measures. The four generator realizations are simulated using Matlab7.0 program. The simulation results show that better performance (*THD%* and Δf are very low or negligible) can be obtained for these realizations by using 32 bits to represent the single-multiplier coefficient and other the outputs of arithmetic operations. The rounding-off method is applied as a quantization process after multiplication process. A comparison is made between one of the best-derived structures and other two recent structures implemented in previous researches. The comparison results indicate that better performance measures can be achieved from the proposed realization for the single-multiplier digital sine-cosine generator.

Keywords: Digital sine-cosine generators, Look-up Table (LUT), CORDIC, Harmonic Distortions, frequency errors, frequency deviation.

تحليل أداء مولدات الجيب والجيب تمام الرقمية أحادية المضرب

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المستخلص:

في هذا البحث, تم اشتقاق تركيب من المرتبة الثانية تمثل مولدات الجيب والجيب تمام الرقمية أحادية المضرب ونتج عنه تحقيقاً لأربعة نماذج مختلفة. إن بَعْض الخصائصِ المهمةِ لهذه المولّدات، مثل نسبة التشويهِ المئويةِ الكليّةِ للتوليف (*THD*%) وخطأ التردد (f_1error) ودقة التردد (Δf) قد تم تعرّيفها وتجريبها كأدوات تقيس. لتحقيق التراكيب الأربعة للمولّدات استعملت المحاكاة ببرنامج Matlab 7.0.وأظهرت نَتائِج المحاكاةَ بأنّ الأداءِ الأفضلِ (قيم *THD%*و Δf منخفضة أَومعدومة) يُمْكِنُ أَنْ يُحْصَلَ عليه لهذه التراكيب استعمال 32 بتلتَمْثي لكل من معاملِا لمضرب الوحيدِ وجميع نواتجِ العملياتِ الحسابيةِ الأخرى. إنّطريقةَ التَدوير قد طبقت في عملية التكميم بعدعمليةِ الضربِ. وعملت مقارنة بين أحد أفضل التراكيبِ المُشْتَقّةِ مع تركيبين آخرين طبّقا في البحوثِ السابقةِ. تُشيرُ نَتائِجُ المقارنةَ إلى أنّ قياسات الأداءِ الأفضل يُمْكِنُ أَن نحصل عليها مِنْ أفضل تركيب مُقتَرَح لمولدات الجيب والجيب تمام الرقمية أحادية المضرب.

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1. Introduction

Digital sine-cosine generators are essential elements in many applications. They are used in communications, music synthesis, control, radar, and digital signal processing [1 - 7]. Stability, flexibility, and low cost are the main advantages of such type of oscillators. Moreover, the parameters of a digitally generated sinusoid are easy to control. A Look-up Table (LUT) is a conventional method for generating desired stable sinusoidal waveforms by storing the amplitude samples in a Read Only Memory (ROM) [l], and read them at appropriate time intervals to produce the desired frequency of sinusoidal waves. Other structures for generating digital sinusoidal waveforms are characterized by using a smaller size ROM [2], or by reducing the harmonic distortion of the sine wave by effectively increasing the table length of the direct LUT method to give high resolution [3]. A second-order recursive digital filter can be used for generating digital sinusoidal waves in a critical unstable mode (poles of the digital transfer function lay on the unit circle in the complex z-plane). Because of the finite word-length constraints that appear in the practical implementation of all recursive digital oscillators, the multiplier coefficient and the outputs of arithmetic operations must be quantized to fit in the allocated word-length causing amplitude distortion and frequency deviation in the generated sinusoidal waves [4 - 5].
A. Abu-El-Haija and M. Al-Ibrahim [6] first reported an improving method for low sensitivity, and low round-off errors performances of digital sinusoidal. A digital sinusoidal oscillator with low and uniform frequency spacing was presented by M. AI-Ibrahim and A. Al-Khateeb[7], but it requires three 14-bit multipliers for its hardware implementation. M. Al-Ibrahim presented then a simple recursive digital sinusoidal oscillator with uniform frequency spacing [8]. Nevertheless, such oscillator structure also required a single 14-bit multiplier for its hardware implementation. Again in 2001, M. Al-Ibrahim [9] introduced a multi-frequency range digital sinusoidal oscillator with high resolution and uniform frequency spacing. He modified this work in 2003 for efficient digital oscillator with continuous phase [10]. Generators based on parallel and pip line CORDICs were also reported [11 - 13]. Recently, a vector rotation approach with recording for the design of sine-cosine synthesizers was accomplished in 2008 by V. Rankovska [14].In this paper,four different realizations of digital sine-cosine oscillators are derived, and evaluated. 32 bits to represent the single-multiplier coefficient and the outputs of arithmetic operations are used. The evaluation results are compared among different derived realizations and between one of the best derived structures and other two recent structures. Such results indicate that better performance measures can be achieved from the proposed realizations.
This paper is organized as follows: Besides this introductory section, Section 2 contains the derivation of different realizations of single-multiplier digital sine-cosine generator. Section 3 describes the simulation results for best realization selection depending on different performance measures. A comparative study is given in Section 4 to show the superiority of such realizations with the use of 32 bits word-length over two recent works. Finally, Section 5concludes this paper.

2. Realizations of Single-Multiplier Digital Sine-Cosine Generator

Different realizations of digital sine-cosine oscillators are considered here. In particular, the derivations of some reduced structures for digital sine-cosine generators that produce the two sinusoidal sequences that are exactly 90 degrees out of phase with each other is first discussed. These circuits have many applications in many signal processing systems such as the computation of the Discrete Fourier Transform (DFT) [8, 9]. They can also form the backbone of certain orthogonal modulation systems utilized in recent optical and mobile communications.

Let $s_1[n]$ and $s_2[n]$ denote the two orthogonal outputs of a digital sine-cosine generator, given by [15]

$$s_1[n] = \alpha \sin(n\theta) \quad \ldots(1)$$

and

$$s_2[n] = \beta \cos(n\theta) \quad \ldots(2)$$

From(1) and (2), it can be written that

$$s_1[n+1] = \alpha \sin((n+1)\theta) = \alpha \sin(n\theta)\cos\theta + \alpha \cos(n\theta)\sin\theta \quad \text{--- (3)}$$

And

$$s_2[n+1] = \beta \cos\big((n+1)\theta\big) = \beta \cos(n\theta)\cos(\theta) - \beta \sin(n\theta)\sin(\theta) \quad \text{--- (4)}$$

Making use of (1) and (2), (3) and (4) can be rewritten in matrix form as

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} \cos\theta & \frac{\alpha}{\beta}\sin\theta \\ -\frac{\beta}{\alpha}\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \ldots(5)$$

So, to obtain $s_1[n]$ and $s_2[n]$ from $s_1[n+1]$ and $s_2[n+1]$, respectively, two delay units are used in the corresponding structure. That is why digital sine-cosine signals can be generated using a second-order recursive digital filter with poles on the unit circle in the complex z-plane [9]. Thus, it is required to compare (5) with the equivalent expression of a general second-order structure with no delay free loops in order to arrive at a realization of the single-multiplier sine-cosine generator. Such second-order structure is characterized by the following equation [15]:

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} 0 & A \\ 0 & 0 \end{bmatrix} \begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} + \begin{bmatrix} C & D \\ E & F \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \ldots(6)$$

Expression (6) can be implemented using five multipliers as shown in Fig. 1 and can be rewritten as in the followings to arrive at the time description of the structure in Fig. 1:

$$s_1[n+1] = A\, s_2[n+1] + D s_2[n] + C s_1[n] \quad \text{--- (7)}$$

and

$$s_2[n+1] = \begin{bmatrix} E & F \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \text{--- (8)}$$

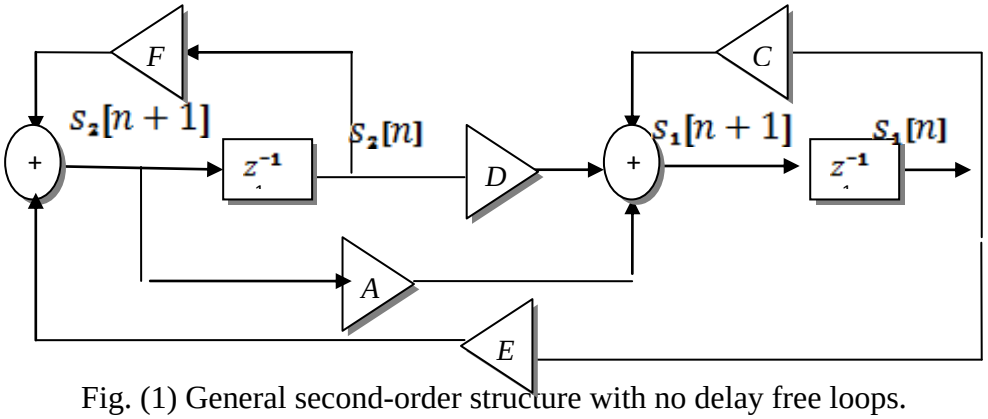

Fig. (1) General second-order structure with no delay free loops.

Substituting (8) into (7), results in

$$s_1[n+1] = (AE + C)s_1[n] + (AF + D)s_2[n] \,.$$

$s_2[n+1]$ can also be derived using the same derivations. Then, in matrix form, it can be formulated as

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} AE + C & AF + D \\ E & F \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \ldots (9)$$

Comparing (5) and (9), yields

$$A = \frac{\alpha(C - cos\theta)}{\beta sin\theta} \quad \text{--- (10)}$$

And

$$D = \frac{\alpha(1 - C.cos\theta)}{\beta sin\theta} \quad \text{--- (11)}$$

Thereby, (6) becomes as follows:

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} 0 & \frac{\alpha(C-cos\theta)}{\beta sin\theta} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} \begin{bmatrix} C & \frac{\alpha(1-C.cos\theta)}{\beta sin\theta} \\ -\frac{\beta}{\alpha} sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \text{--- (12)}$$

It can be seen that, (12) requires five multipliers for implementation. The number of multipliers can be reduced by substituting specific values for the constant *C*. This will be discussed in the following subsections:

2.1 A Single-Multiplier Sine-Cosine Generator BySetting $C = cos\theta$

By Setting ($C = cos\theta$), (12) can be rewritten as

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} cos\theta & \frac{\alpha}{\beta} sin\theta \\ -\frac{\beta}{\alpha} sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \ldots (13)$$

Equation (13) requires four multipliers to be implemented. This number can further be reduced to a single multiplier by setting ($\frac{\beta}{\alpha} sin\theta = 1 - cos\theta$) or equivalently ($\beta = \alpha \tan\left(\frac{\theta}{2}\right)$), thus

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} cos\theta & cos\theta + 1 \\ cos\theta - 1 & cos\theta \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \ldots (14)$$

The matrix form in (14) can lead to the realization of Fig. 2, where Q is the quantization process on the multiplier output. The output frequency (f) depends on $(cos\theta)$ input and sample clock rate ($R_1 clk$) according to the following equation [8]:

$$f = \frac{R_{clk}.\theta}{360} \frac{cycles}{second} \quad \ldots (15)$$

From (15), it can be seen that as $(cos\theta) \to 1$, then $\theta \to 0$ and $f \to 0$. Peak amplitude of digital cosine $s_2[n]$ is always one, while peak amplitude of digital sine $s_1[n]$ can be computed according to the following equation:

$$Peak_{Amp} of\ s_1[n] = \frac{cos\theta + 1}{sin\theta} \quad \text{---- (16)}$$

with

$$Peak_{Amp}\,of\;\; s_2[n] = 1 \qquad \text{---- (17)}$$

So, as $(cos\theta) \rightarrow 1$, then $sin\theta \rightarrow 0$ and $eak_{Amp}\,of\; s_1[n] \rightarrow \infty$

Thus, from (15) and (16), the peak amplitude of $s_1[n]$ in a particular implementation is a functionθ which can be set by the minimum output frequency ($f_1 min$) and the clock rate ($R_1 clk$) as

$$Peak_{Amp}\,of s_1[n] = \frac{\cos\left(\frac{360.f_{min}}{R_{clk}}\right) + 1}{sin\left(\frac{360.f_{min}}{R_{clk}}\right)} \qquad \text{---- (18)}$$

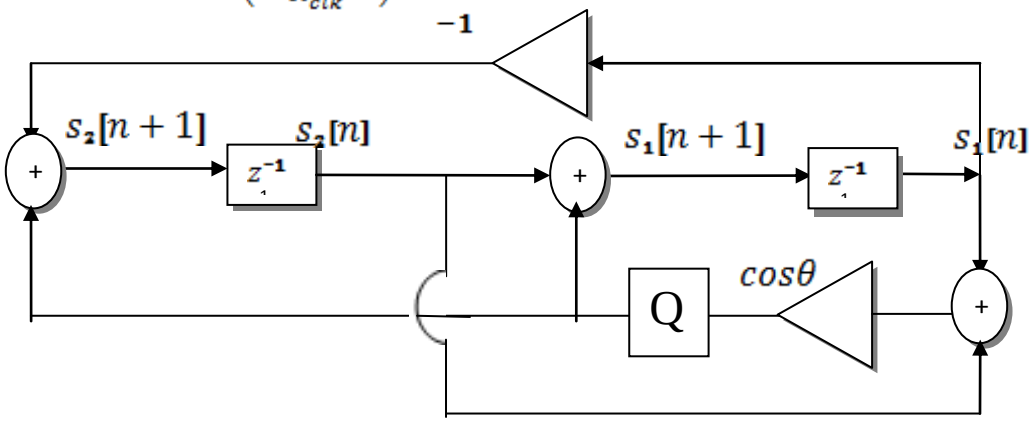

Fig. (2) A single-multiplier sine-cosine generator by setting ($C = cos\theta$).

Another single-multiplier sine-cosine generator can be derived from (13) by setting

$-\frac{\beta sin\theta}{\alpha} = 1 + cos\theta$ or equivalently ($\alpha = \beta \tan\left(\frac{\theta}{2}\right)$). Then

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} cos\theta & cos\theta - 1 \\ cos\theta + 1 & cos\theta \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \qquad \text{---- (19)}$$

The realization of (19) is illustrated in Fig.3 with an alternate single-multiplier structure.

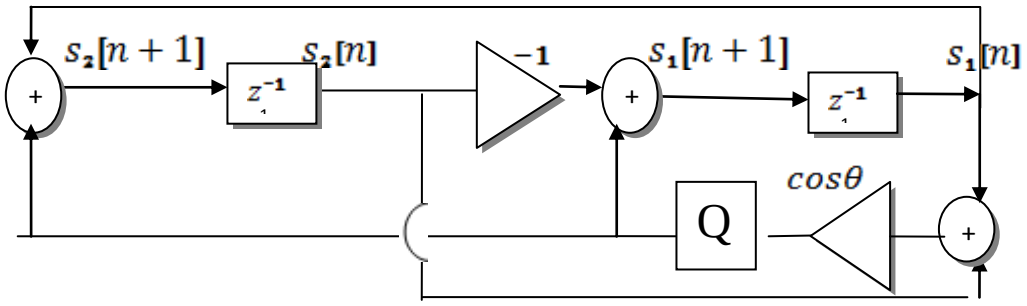

Fig. (3), A single-multiplier sine-cosine generator by setting ($\frac{\beta}{\alpha} = -\frac{1 + cos\theta}{sin\theta}$).

2.2 A Single-Multiplier Sine-Cosine Generator By Setting *C*=0

Another realization of the single-multiplier sine-cosine generator can be obtained by setting another specific value for the multiplier constant (C). That is C=0.Therefore, (12) can be reduced to

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} 0 & \frac{-\alpha cos\theta}{\beta sin\theta} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} + \begin{bmatrix} 0 & \frac{\alpha}{\beta sin\theta} \\ -\frac{\beta}{\alpha} sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \ldots (20)$$

From (20), multiple realizations with single-multiplier can be achieved by choosing appropriate values for the two variables$(\alpha \text{and} \square)$;such as choosing $\alpha = \beta sin\theta$, then (20) can be written as

$$\begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} = \begin{bmatrix} 0 & -cos\theta \\ 0 & 0 \end{bmatrix} \begin{bmatrix} s_1[n+1] \\ s_2[n+1] \end{bmatrix} + \begin{bmatrix} 0 & 1 \\ -1 & cos\theta \end{bmatrix} \begin{bmatrix} s_1[n] \\ s_2[n] \end{bmatrix} \quad \ldots (21)$$

It is worth-mentioning thatthe realization of (21) can be accomplished with two multipliers ($cos\theta$ and $-cos\theta$. It can be modified to yield a single-multiplier realization as shown in Fig. 4. Equivalent structures to that shown in Fig. 4 can also be derived by setting $C = 0$ and choosing $\alpha = -\beta sin\theta$ or by setting $C = 1$ and choosing $\alpha = \beta sin\theta$.

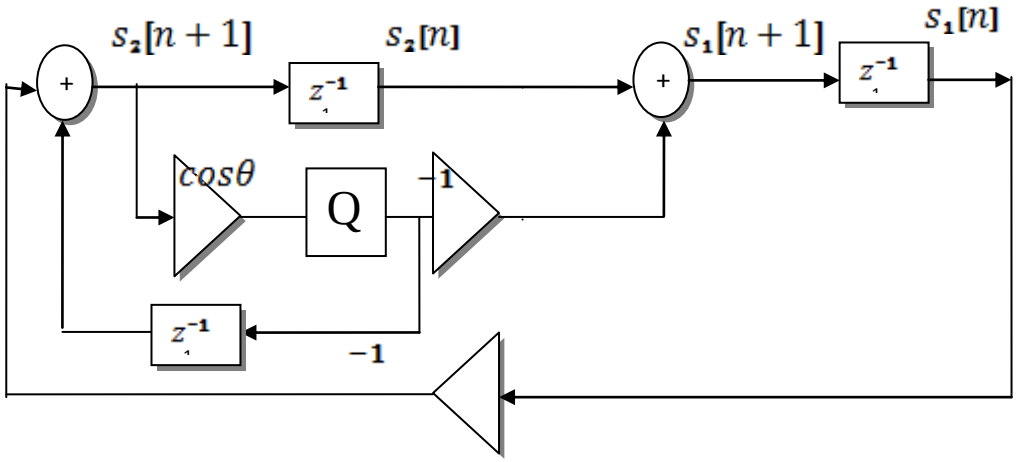

Fig. (4), A single-multiplier sine-cosine generator by setting ($C = 0$ and $\alpha = \beta sin\theta$).

2.3 General Form for The Second-Order Difference Equation

As mentioned before, digital sinusoidal signals can be generated using a second-order recursive digital filter with poles on the unit circle in the complex z-plane. The difference equation of the critical unstable digital system representing the direct form digital sine wave oscillator contains one multiplication operation and one subtraction and can be derived as follows [6, 9]:

Let the generator output be $y(n) = sin\omega_0 n$. Then

$$y(n-1) = sin\omega_0(n-1) \quad \text{---- (22)}$$

and

$$y(n-2) = sin\omega_0(n-2) \qquad \text{---- (23)}$$

From the homogenous equations, the difference equation of second order can be written as follows:

$$y(n) = 2cos\theta\, y(n-1) - y(n-2) \qquad for \;\; n \geq 0 \qquad \text{---- (24)}$$

The corresponding block diagram representation of (24) is shown in Fig. 5. To generate the digital sine-cosine wave, initial values of the variable $y(n)$ must be chosen so that the first samples take amplitudes of zero and one for sine and cosine waves, respectively. One of these initials should not be a zero. A zero value is chosen as an initial for the output sine wave $s_1[n] = 0$, since it starts with zero at $n = 0$. While $s_2[n] = 1$ at $n = 0$ is chosen as another initial, since it is a cosine wave. Other amplitudes of the rest samples are generated subsequently according to the previous selected values. For example, if the generator input has an angle (θ), then the initial values of $y(-1)$ must be equal to $\sin(-\theta)$ and $y(-2)=\sin(-2\theta)$ and the output is a sine wave$s_1[n]$. On the other hand, to generate a cosine wave $s_2[n]$, the initial values of $y(-1)$ must be changed to $\cos(-\theta)$ and $y(-2)=\cos(-2\theta)$.

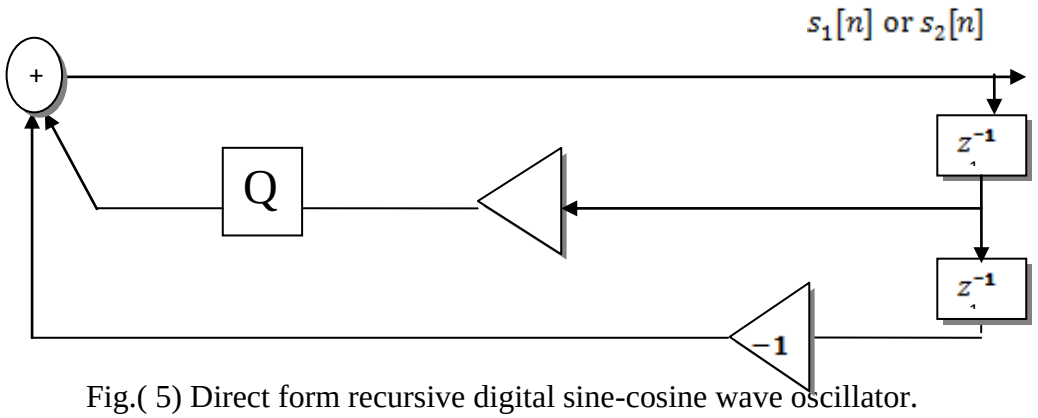

Fig.(5) Direct form recursive digital sine-cosine wave oscillator.

In all previous structures, it should be noted that to start the generation of the sinusoidal sequences, one of the signal variables $s_1[n]$, $s_2[n]$ should at least be initially set to a nonzero value. Moreover, the actual amplitudes and the relative phases of the sinusoidal and the cosinusoidal sequences generated by the sine-cosine generator depend on the initial values chosen for the signal variables $s_1[n]$ and $s_2[n]$. It should also be noted that the maximum value of the amplitudes of these two sequences can be made equal by amplitude scaling one of the sequences appropriately.

Single-multiplier structures for sine-cosine generators have many advantages over other structures with many multipliers, such as that the single-multiplier structures retain their characteristic roots on the unit circle under finite word-length constraints. On the other hand, in other realizations of the sine-cosine generators, roots may go inside or outside the unit circle due to the quantization of the multiplier coefficients, causing the oscillations to decay or to build up as n increase. In addition, due to product round-off errors, the sequences generated by the sine-cosine generator may not retain their sinusoidal behaviors, even in the case of a single-multiplier generator [7 - 10]. It is therefore advisable to reset the variables $s_1[n]$ and $s_2[n]$ after some iterations at prescribed time instants, so that the accumulated errors do not become unacceptable. The other advantages of such structures are reducing the

chip area used when implemented in hardware, while increasing the speed of such implementations.

In all above-mentioned oscillators, it can also be seen that the desired angle $\theta = \theta_d$ represented by the oscillator coefficient ($\cos\theta = \cos\theta_d$) is related to the oscillator frequency by

$$\theta_d = \omega_d T = 2\pi f_d T \quad \text{---- (24)}$$

Where ω_d is the desired angular frequency of the generated sinusoid in radians per second, f_d is the desired frequency in cycles per second, and *T* is the time interval between two consecutive samples of the generated sinusoidal waveform (*i.e.*, the sampling interval). It is also convenient to consider the desired number of samples in a complete cycle of the sinusoidal waveform as

$$N = \frac{2\pi}{\theta_d} \quad \text{... (26)}$$

Therefore, the smallest frequency which the oscillator can generate is

$$f_{min} = \frac{\theta_{min}}{2\pi}\frac{1}{T} \quad \text{... (27)}$$

or equivalently, the maximum number of samples per cycle is

$$N_{max} = \frac{2\pi}{\theta_{min}} \quad \text{... (28)}$$

Where θ_{min} is the minimum desired angle.

3. Simulation Results for Best Realization Selection

Three important characteristics are used to measure the performance of the designed oscillators. The first characteristic is the percentage of the Total Harmonic Distortion (*THD%*) which is the ratio of energy in the harmonics to the total energy of the signal [1]. $s_1[n]$ or $s_2[n]$ signals can be treated as a periodic discrete time sequence $x(n)$, the calculation of *THD%* takes the form of [8]

$$THD\% = \frac{E_t - E(f_0)}{E_t} \times 100\% \quad \text{... (29)}$$

where

$$E_t = \frac{1}{N}\sum_{k=0}^{N-1}|X(k)|^2 \quad \text{... (30)}$$

and

$$E(f_0) = \frac{2}{N}|X(k_0)|^2 \quad \text{... (31)}$$

N is the number of samples in an integer number of periods, E_t is the total energy of the waveform, $E(f_0)$ is the energy of the fundamental frequency f_0, $X(k)$ is the Discrete Fourier Transform (DFT) of $x(n)$ and k_0 is the DFT index which is related to the fundamental frequency by

$$k_0 = N f_0 T \quad \text{---- (32)}$$

The second characteristic of a digital oscillator is the frequency error ($f_1 error$) given by [8]

$$f_{error} = absolute\ (f_d - f_g) \quad \text{---- (33)}$$

where f_{error} is the deviation of the generated frequency from the ideal frequency which resulted from nonlinear behavior of the oscillator, f_d is the desired (ideal) frequency of the wave without error and f_g is the frequency generated by an oscillator structure through the multiplication process of the signal with coefficient $cos\theta$ as in Figs. 2, 3, 5 and 6.

The last characteristic of digital oscillators, to be examined in this paper, is the frequency deviation (Δf) . It is defined as the difference between two consecutive frequencies. The frequency deviation (Δf) is a measure of claimed uniform frequency spacing and is defined by [8]

$$\Delta f = \frac{f(\theta) - mf(\theta_{min})}{f(\theta_{min})} \quad \text{---- (34)}$$

Where. M= $\frac{\theta_{max}}{\theta}$

It should be noted that, a small frequency deviation is required for a practically usable digital oscillator. The performance measures that are mentioned can be used to describe the efficiency of different single-multiplier digital sine-cosine generators in Figs. 2, 3, 5 and 6 for the selected word-length size of 32 bits. The generators are simulated using Matlab7.0 program and the results are presented in Tables 1-8. The simulation results are obtained assuming a total of 32 bits word-length size for both arithmetic sign and magnitude number representation. The rounding-off quantization process is performed on the result of multiplication process and the initial values are chosen such that $s_1[0] = 0$ and $s_2[0] = 1$. Tables 1-8 give the values of different angles along with the number of samples per cycle of the generated sinusoidal and co-sinusoidal signalsN_g . The frequency of the generated sinusoidal and co-sinusoidal signals $f_d(\theta)$and the frequency deviations $\Delta f_d(\theta)$ are calculated assuming a clock frequency of f_{clk} = 50MHzand presented in these tables. The frequency deviation $\Delta f_d(\theta)$is a measure of the claimed uniform frequency spacing and is specified by (45). The total harmonic distortion percentage *THD%* and frequency errorf_{error} described by (40) and (44), respectively are also presented in Tables 1-8.

From such tables, it can be seen that the maximum value of *THD%* is obtained when the input angle to the generators is 0.0014649536460638 radian. The maximum values of f_{error} are produced when the input angle is 0.0014649536460638radian for sine waves but are different for different input angle values for cosine waves. The values of f_{error} for cosine waves are greater than those for sine waves. The values of Δf are the same for sine and cosine waves for all input angle values. Also, it can be seen that the maximum values of *THD%*, f_{error} *(sine)* and Δf are of the same order, while the maximum value of f_{error} (*cosine*) is 16.5312Hz for the realization of Fig. 5. The minimum value of f_{error} (*sine*) is 0Hz for the realization of Fig. 5. Thus, one can conclude that Fig. 5 is the best realization from the point of view of output errors for different angles.

4. A Comparative Study

It should be noted that the structures in Figs. 2, 3, 4 and 5 are realized using a word-length size of 32 bits. A comparison is made between the structure in Fig. 5 and other structures implemented in previous researches given in *Refs.*[8] & [9]. The comparison indicates that

better performance measures can be achieved from Fig. 5 using the word-length size of 32 bits and rounding-off method as a quantization process after multiplication process. Tables 9 and 10 show the comparison results for the structure in Fig. 5 with those of *Refs*. [8] & [9]. The simulation results and performance measures indicate that *THD%* and Δf are very low or neglected in the case of the proposed structure in Fig. 5.

It should also be noted that the structure in *Ref.* [8] uses one multiplier for realization and number of bits used to represent the coefficients and variables is 11 bits. The quantization method used after the multiplication process is rounding. While, the structure in *Ref.* [9] uses two multipliers each with 8 bits and two integrators each with 15 bits for realization to give digital sine-cosine wave.

To investigate the effect of word-length size variation, the resulting *THD%* and $f_{error}\ (sine)$ in the sinusoidal output of the structure of Fig. 5 are shown, respectively in Figs. 6 and 7 for different θ 's and different bit representations (8, 12, 16, 24 and 32 bits)with a clock frequency of 50MHz. From Figs. 6 and 7, it can be noticed that the performance superiority of the 32-bit representation is guaranteed.

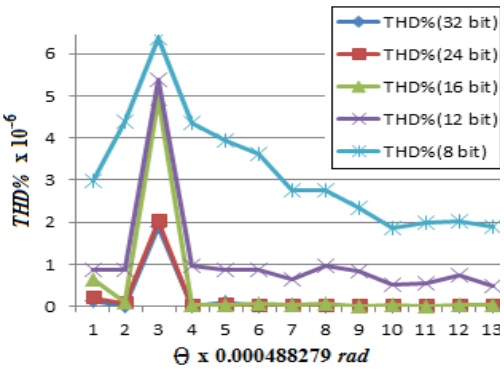

Fig. 6 Total harmonic distortion percentage *THD%* for sine wave.

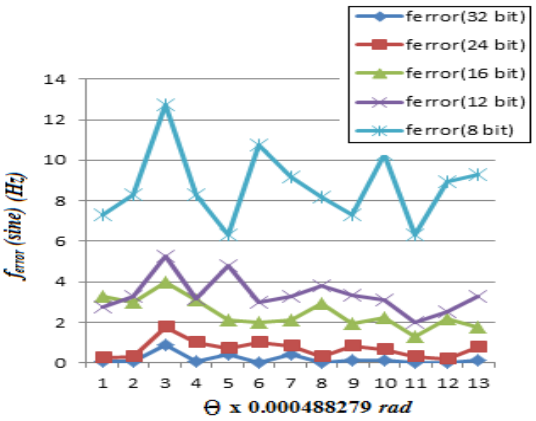

Fig.7 Absolute frequency errorf_{error} *(sine)* for sine wave.

Table 1: Parameters of the structure in Fig. 2 and the generated sine signal $s_1[n]$ for. f_{clk}=50MHz

Angle (θ) in radian (32 bits representation)	N_g	*THD% (sine)* $\times 10^{-6}$	f_{error} *(sine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0.0011	0.2759	0
0.0210139974951744	299	0.0001	0.1397	0.5026
0.0185893047600985	338	0.0010	0.1223	2.0107
0.0146803390234709	428	0.0001	0.0002	1.0053
0.0122240968048573	514	0.0005	0.0640	-2.0107
0.00781490653753281	804	0.0014	0.1054	1.0053
0.0058611799031496	1072	0.0027	0.1062	1.0053
0.0039074532687664	1608	0.0013	0.0544	0.5026
0.00293059088289738	2144	0.1247	0.4346	-1.0053
0.00195311941206455	3217	0.0188	0.1056	0.5026
0.0014649536460638	4289	1.9500	0.8841	-0.5026
0.000976560637354851	6434	0.0434	0.0862	-2.0107
0.000488279387354851	12868	0.1058	0.0596	1.0053

Table 2: Parameters of the structure in Fig. 2 and the generated cosine signal $s_2[n]$ for f_{clk}=50MHz.

Angle (θ) in radian (32 bits representation)	N_g	*THD% (cosine)* $\times 10^{-6}$	f_{error} *(cosine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0.0025	148.2497	0
0.0210139974951744	299	0.0010	0	0.5026
0.0185893047600985	338	0.0006	79.6889	2.0107
0.0146803390234709	428	0.0010	0	1.0053
0.0122240968048573	514	0.0023	30.2476	-2.0107
0.00781490653753281	804	0.0018	27.3508	1.0053
0.0058611799031496	1072	0.0024	29.0152	1.0053
0.0039074532687664	1608	0.0021	19.3434	0.5026
0.00293059088289738	2144	0.0983	27.1559	-1.0053
0.00195311941206455	3217	0.0176	9.6687	0.5026
0.0014649536460638	4289	1.4028	16.2287	-0.5026
0.000976560637354851	6434	0.0347	6.3965	-2.0107
0.000488279387354851	12868	0.07860	2.4171	1.0053

Table 3: Parameters of the structure in Fig. 3 and the generated sine signal $s_1[n]$ for . f_{clk}=50MHz

Angle (θ) in radian (32 bits representation)	N_g	*THD% (sine)* $\times 10^{-6}$	f_{error} *(sine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0.0001	0.1062	0
0.0210139974951744	299	0	0.0235	0.5026
0.0185893047600985	338	0	0.0070	2.0107
0.0146803390234709	428	0.0004	0.1274	1.0053
0.0122240968048573	514	0.0004	0.1038	2.0107
0.00781490653753281	804	0.0003	0.0542	1.0053
0.0058611799031496	1072	0.0264	0.4057	1.0053
0.0039074532687664	1608	0.0045	0.1038	0.5026
0.00293059088289738	2144	0.1078	0.3963	-1.0053
0.00195311941206455	3217	0.0051	0.0684	0.5026
0.0014649536460638	4289	1.8296	0.8305	-0.5026
0.000976560637354851	6434	0.1183	0.0684	-2.0107
0.000488279387354851	12868	0.3998	0.1509	1.0053

Table 4: Parameters of the structure in Fig. 3 and the generated cosine signal $s_2[n]$ for . f_{clk}=50MHz

Angle (θ) in radian (32 bits representation)	N_g	*THD% (cosine)* $\times 10^{-6}$	f_{error} *(cosine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0	11.8785	0
0.0210139974951744	299	0	26.6467	0.5026
0.0185893047600985	338	0	1.7599	2.0107
0.0146803390234709	428	0.0003	18.1244	1.0053
0.0122240968048573	514	0.0003	18.1797	2.0107
0.00781490653753281	804	0.0001	12.8958	1.0053
0.0058611799031496	1072	0.0194	12.9778	1.0053
0.0039074532687664	1608	0.0031	13.3303	0.5026
0.00293059088289738	2144	0.0650	14.3973	-1.0053
0.00195311941206455	3217	0.0004	4.4558	0.5026
0.0014649536460638	4289	1.2834	6.3166	-0.5026
0.000976560637354851	6434	0.1020	16.2681	-2.0107
0.000488279387354851	12868	0.4281	2.1410	1.0053

Table 5: Parameters of the structure in Fig. 4 and the generated sine signal $s_1[n]$ for f_{clk} =50MHz

Angle (θ) in radian (32 bits representation)	N_g	*THD% (sine)* $\times 10^{-6}$	f_{error} *(sine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0	0.1015	0
0.0210139974951744	299	0	0.0212	0.5026
0.0185893047600985	338	0	0.0188	2.0107
0.0146803390234709	428	0.0004	0.1274	1.0053
0.0122240968048573	514	0.0002	0.0778	-2.0107
0.00781490653753281	804	0.0002	0.0471	1.0053
0.0058611799031496	1072	0.0230	0.3939	1.0053
0.0039074532687664	1608	0.0024	0.0802	0.5026
0.00293059088289738	2144	0.1039	0.4175	-1.0053
0.00195311941206455	3217	0.0096	0.0636	0.5026
0.0014649536460638	4289	1.9163	0.8517	-0.5026
0.000976560637354851	6434	0.0224	0.0660	-2.0107
0.000488279387354851	12868	0.4123	0.1533	1.0053

Table 6: Parameters of the structure in Fig. 4 and the generated cosine signal $s_2[n]$ for f_{clk} =50MHz.

Angle (θ) in radian (32 bits representation)	N_g	*THD% (cosine)* $\times 10^{-6}$	f_{error}*(cosine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0	18.2761	0
0.0210139974951744	299	0	24.7194	0.5026
0.0185893047600985	338	0	21.3170	2.0107
0.0146803390234709	428	0.0002	23.2614	1.0053
0.0122240968048573	514	0.0001	19.9825	-2.0107
0.00781490653753281	804	0.0001	14.1965	1.0053
0.0058611799031496	1072	0.0211	13.7092	1.0053
0.0039074532687664	1608	0.0016	7.13675	0.5026
0.00293059088289738	2144	0.0755	3.1148	-1.0053
0.00195311941206455	3217	0.0138	9.3566	0.5026
0.0014649536460638	4289	1.3750	6.0846	-0.5026
0.000976560637354851	6434	0.0268	4.8485	-2.0107
0.000488279387354851	12868	0.4085	3.2965	1.0053

Table 7: Parameters of the structure in Fig. 5 and the generated sine signal $s_1[n]$ for f_{clk} =50MHz

Angle (θ) in radian (32 bits representation)	N_g	*THD% (sine)* $\times 10^{-6}$	f_{error} *(sine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0	0.1002	0
0.0210139974951744	299	0	0.0282	0.5026
0.0185893047600985	338	0	0	2.0107
0.0146803390234709	428	0.0004	0.1272	1.0053
0.0122240968048573	514	0.0004	0.1011	2.0107
0.00781490653753281	804	0	0.0214	1.0053
0.0058611799031496	1072	0.0244	0.3870	1.0053
0.0039074532687664	1608	0	0.0171	0.5026
0.00293059088289738	2144	0.1174	0.4259	-1.0053
0.00195311941206455	3217	0.0045	0.0579	0.5026
0.0014649536460638	4289	1.9092	0.8537	-0.5026
0.000976560637354851	6434	0.0110	0.0439	-2.0107
0.000488279387354851	12868	0.1341	0.0659	1.0053

Table 8: Parameters of the structure in Fig. 5 and the generated cosine signal $s_2[n]$ for f_{clk}=50MHz

Angle (θ) in radian (32 bits representation)	N_g	*THD% (cosine)* $\times 10^{-6}$	f_{error}*(cosine) (Hz)*	Δf $\times 10^{-6}$
0.0244481917470694	257	0	16.5312	0
0.0210139974951744	299	0	2.5684	0.5026
0.0185893047600985	338	0	4.3110	2.0107
0.0146803390234709	428	0.0003	13.5244	1.0053
0.0122240968048573	514	0.0002	6.1606	-2.0107
0.00781490653753281	804	0	10.5520	1.0053
0.0058611799031496	1072	0.0180	8.6813	1.0053
0.0039074532687664	1608	0.0009	10.955	0.5026
0.00293059088289738	2144	0.0688	4.1347	-1.0053
0.00195311941206455	3217	0.0028	4.2191	0.5026
0.0014649536460638	4289	1.3916	4.9713	-0.5026
0.000976560637354851	6434	0.0083	9.4770	-2.0107
0.000488279387354851	12868	0.0938	6.1869	1.0053

Table 9: A comparison with the previous implementation of *Ref.*[8]for f_{clk}=50MHz

Angle (θ) in radian (32 bits representation)	N_g	THD_p% $\times 10^{-6}$	THD_8% $\times 10^{-6}$	Δf_p $\times 10^{-6}$	Δf_8 $\times 10^{-2}$
0.0244481917470694	257	0	8.61	0	0.583
0.0210139974951744	299	0	10.04	0.5026	0.332
0.018589305691421	338	0	8.913	2.0107	0.237
0.0146803399547935	428	0.0004	6.92	1.0053	0.045
0.0122240958735347	514	0.0004	7.73	-2.0107	0.0
0.00781490746885538	804	0	7.601	1.0053	0.02
0.0058611799031496	1072	0.0244	6.384	1.0053	0.004
0.0039074532687664	1608	0	6.179	0.5026	0.0
0.0029305899515748	2144	0.1174	5.907	-1.0053	0.0
0.00195311941206455	3217	0.0045	5.981	0.5026	0.0
0.0014649536460638	4289	1.9092	5.95	-0.5026	0.0
0.000976559706032276	6434	0.0110	5.594	-2.0107	0.0
0.000488280318677425	12868	0.1341	5.7	1.0053	0.0

THD_p% and THD_8% are the total harmonic distortion percentage for the proposed and *Ref.*[8], respectively.Δf_p and$\Delta f_8$are the frequency resolution for the proposed structure in Fig. 5 and that in*Ref.*[8], respectively.

Table 10:A comparison with the previous implementation of*Ref.*[9]for f_{clk}= 50MHz .

Angle (θ) in radian (32 bits representation)	N_g	THD_p% $\times 10^{-7}$	THD_9% $\times 10^{-7}$	Δf_p $\times 10^{2}$	Δf_9 $\times 10^{2}$
0.0442477837204933	142	0	10.838	0	0.3159
0.039269907400012	160	0	9.059	0	0.2487
0.0455303285270929	138	0	5.575	0	0.136
0.0312596280127764	201	0.0005	2.085	0	0.1105
0.0293606799095869	214	0	5.105	0	0.0717
0.024448191747069	257	0.0009	3.153	0	0.0278
0.0195737853646278	321	0.0043	3.229	0	0.0
0.0146803390234709	428	0.0042	2.730	0	0.0
0.00977167300879955	643	0.0002	1.707	0	0.0
0.0048858355730772	1286	0.1611	1.675	0	0.0
0.0039074532687664	1608	0.0009	1.652	0	0.0
0.00293059088289738	2144	1.1742	1.279	0	0.0
0.00195311941206455	3217	0.0451	1.660	0	0.0
0.000976560637354851	6434	0.1105	1.638	0	0.0

$THD_p\%$ and THD_9 % are the total harmonic distortion percentage for the proposed and *Ref.*[9], respectively. Δf_p and Δf_9 are the frequency resolution for the proposed structure in Fig. 5 and that in *Ref.*[9], respectively.

5. Conclusions

Four realizations of single-multiplier digital sine-cosine generators have been presented form second order structure. It has been shown that the proposed realizations can generate $THD\%$, f_{error} and Δf much lower than those generated by previous works for a 32-bit word-length of the multiplier coefficient and all outputs of arithmetic operations. The proposed generators have required only one multiplier for their implementations, means that one quantization process is to be done after multiplication process. Therefore, it can be concluded that the implemented digital oscillators exhibit superior performance compared with the oscillators in *Refs.* [8] and [9]. In addition, the proposed generators have the advantage of uniform frequency spacing which makes it suitable for modern communication applications.

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